Michael Flynn Seminar

Progress in Integrated Analog-Digital Interfaces

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Michael P. Flynn received the Ph.D. degree from Carnegie Mellon University in 1995. He received the B.E. and M.Eng.Sc. degrees from University College Cork, Ireland in 1988 and 1990, respectively. From 1988 to 1991 he was with the National Microelectronics Research Centre in Cork, Ireland. He was with National Semiconductor in Santa Clara, CA, from 1993 to 1995 and from 1995 to 1997 he was a Member of Technical Staff with Texas Instruments, Dallas, TX. During the four-year period from 1997 to 2001, he was with Parthus Technologies, Cork, Ireland. Dr. Flynn joined the University of Michigan in 2001 and is currently Professor. His technical interests are in data conversion, RF circuits, serial transceivers and biomedical systems.

Michael Flynn is an IEEE Fellow and a 2008 Guggenheim Fellow. He has served on the Technical Program Committees of the International Solid State Circuits Conference (ISSCC), the Symposium on VLSI Circuits and the Asian Solid-State Circuits Conference (ASSCC) and the European Solid-State Circuits Conference. He was a Distinguished Lecturer of the IEEE Solid-State Circuits Society. He was Editor-in-Chief of the IEEE Journal of Solid-State Circuits from 2013 to 2016.

The analog-digital interface is an essential part of sensing, communication and data-storage systems. New techniques are driving continued improvements in the efficiency and capability of Analog to Digital Converters (ADCs). The last fifteen years has seen a remarkable three order-of-magnitude improvement in ADC energy efficiency. This is in part due to CMOS technology scaling, however new architectures and new circuit ideas are responsible for much of this improvement. At the same time, new techniques are enhancing analog-digital interfaces, enabling new applications such as simultaneous neural recording and stimulation for treatment of epilepsy, and delivering new capabilities such as machine learning for sensors.

The first part of the presentation will review CMOS ADC architectures and introduce some new techniques. Important architectures such as successive approximation and pipeline are more that 50 years old. On the other hand, recent advances allow ADCs to be based on CMOS inverters. Other new ADCs directly digitize high frequency RF signals.

As an example of an ADC based system, a new ADC-based correlator system facilitates Geostar, a next generation weather satellite. GeoSTAR is a new type of microwave sounder that will produce three-dimensional images of tropospheric temperature and humidity profiles of the Earth from geostationary orbit (GEO) every 15 to 30 minutes. Leveraging the performance and efficiency of the analog-digital interface, a prototype mixed-signal correlator IC has 128 high speed (1GHz) ADCs and the extensive DSP.

A bi-directional neural interface chip employs stimulation artifact cancellation within the analog-digital interface to facilitate concurrent neural recording and stimulation. This capability significantly improves the performance of brain machine interfaces for treatment of diseases such as epilepsy. The device uses common average referencing (CAR) to suppress cross-channel common-mode noise. A range-adapting (RA) successive approximation ADC is very energy efficient. The fabricated prototype consumes only 330 nW per channel.

Internet of Things (IoT) devices are collecting and transmitting an ever-increasing amount of data to monitor health, the environment and manufacturing. Machine learning can overcome bandwidth and power limitations by decreasing the amount of transmitted data through feature extraction, or classification at the sensor. A challenge is that these need energy intensive and accurate inner-product multiplication of the input signal with a basis vector. A compelling approach is to embed machine learning functions within the digitization process. Our new approach achieves a classification accuracy equivalent to floating point DSP by embedding the inner-product calculation within an ADC array. The prototype chip recognizes hand-written digits as accurately as a conventional DSP implementation.

A digital-analog hybrid neural network exploits efficient analog computation and digital intra-network communication for feature extraction and classification. Taking advantage of the inherently low SNR requirements of the Locally Competitive Algorithm (LCA), the internally-analog neuron is 3x smaller and 7.5x more energy efficient than an equivalent digital design. This work demonstrates large-scale integration of 512 analog neurons using a traditional scalable digital workflow to achieve a best-of-class power efficiency of 3.43TOPS/W for object classification. At 48.9pJ/pixel and 50.1nJ/classification, the prototype 512-neuron IC achieves 2x efficiency over the digital design while maintaining reliable classification results over PVT.